What is claimed is:

1. A digital phase lock loop circuit comprising:

an error generation circuit for generating at least three error signals; and,

a phase error adjustment circuit for generating at least one phase error adjustment signal from the at least three error signals.

2. The digital phase lock loop circuit of claim 1, wherein the at least three error signals comprise:

at least one first error signal, said first error signal corresponding to an error between a first sampled value and a first ideal value;

at least one second error signal, said second error signal corresponding to an error between a second sampled value, slightly ahead of the first sampled value in time, and the first ideal value; and,

at least one third error signal, said third error signal corresponding to an error between a third sampled value, slightly behind the first sampled value in time, and the first ideal value.

3. The digital phase lock loop circuit of claim 1, wherein the at least three error signals comprise:

at least one first error signal, said first error signal corresponding to an error between a first sampled value and a first ideal value;

at least one second error signal, said second error signal corresponding to an error between a first interpolated sample value, slightly ahead of the first sampled value in time, and the first ideal value; and,

at least one third error signal, said third error signal corresponding to an error between a second interpolated sample value, slightly behind the first sampled value in time, and the first ideal value.

4. The digital phase lock loop circuit of claim 1, wherein the at least three error signals comprise:

at least one first error signal, said first error signal corresponding to an error between a first sampled value and a first ideal value;

at least one second error signal, said second error signal corresponding to an error between the first sampled value and a second ideal value which is slightly ahead of the first ideal value in time; and,

at least one third error signal, said third error signal corresponding to an error between the first sampled value and a third ideal value which is slightly behind the first ideal value in time.

5. The digital phase lock loop circuit of claim 1, wherein the at least one phase error adjustment signal specifies at least direction of phase drift for a signal.

6. The digital phase lock loop circuit of claim 4, wherein the at least one first error signal is produced by taking the difference between a first digital output signal and a second digital output signal.

7. The digital phase lock loop circuit of claim 6, wherein the at least one second error signal is produced by taking the difference between the first digital output signal and a phase shifted version of the second digital output signal, said phase shift being in a positive direction.

8. The digital phase lock loop circuit of claim 6, wherein the at least one second error signal is produced by taking the difference between the first digital output signal and a phase shifted version of the second digital output signal, said phase shift being in a negative direction.

9. The digital phase lock loop circuit of claim 1, wherein the at least one phase error adjustment signal comprises at least three signals including:

at least one drift direction signal

at least one drift duration signal; and

at least one drift amount signal.

10. A read channel device comprising:

an error generation circuit for generating at least three error signals; and,

a phase error adjustment circuit for generating at least one phase error adjustment signal from the at least three error signals.

11. A data storage system comprising:

a data storage assembly;

a read channel device operable to read information stored on the data storage assembly, said read channel device comprising an error generation circuit for generating at least three error signals; and, a phase error adjustment circuit for generating at least one phase error adjustment signal from the at least three error signals.

12. The data storage system of claim 11, wherein said data storage assembly comprises a hard disk drive.

13. A method for determining and correcting a phase error, comprising the steps of:

generating at least three error signals; and,

generating at least one phase error adjustment signal from the at least three error signals.

14. The method of claim 13, wherein the step of generating at least three error signals comprises:

generating at least one first error signal, said first error signal corresponding to an error between a first sampled value and a first ideal value;

generating at least one second error signal, said second error signal corresponding to an error between the first sampled value and a second ideal value which is slightly ahead of the first ideal value in time; and,

generating at least one third error signal, said third error signal corresponding to an error between the first sampled value and a third ideal value which is slightly behind the first ideal value in time.

15. The method of claim 13, wherein the step of generating at least one phase error adjustment signal comprises:

generating at least one at least one drift direction signal.

16. The method of claim 15, wherein the step of generating at least one phase error adjustment signal comprises the further steps of:

generating at least one drift duration signal; and,

generating at least one drift amount signal.

17. The method of claim 13, wherein the step of generating at least one phase error adjustment signal comprises:

generating at least one first summation error signal by taking the sum of a plurality of the at least one first error signals;

generating at least one second summation error signal by taking the sum of a plurality of the at least one second error signals; and,

generating at least one third summation error signal by taking the sum of a plurality of the at least one third error signals.

18. The method of claim 13, wherein the step of generating at least one phase error adjustment signal comprises:

generating at least one first summation error signal by taking the root mean square of a plurality of the at least one first error signals;

generating at least one second summation error signal by taking the root mean square of a plurality of the at least one second error signals; and,

generating at least one third summation error signal by taking the root mean square of a plurality of the at least one third error signals.

19. The method of claim 13, wherein the step of generating at least one phase error adjustment signal comprises:

generating at least one first summation error signal by taking the sum of the squares of a plurality of the at least one first error signals;

generating at least one second summation error signal by taking the sum of the squares of a plurality of the at least one second error signals; and,

generating at least one third summation error signal by taking the sum of the squares of a plurality of the at least one third error signals.

20. The method of claim 13, wherein the step of generating at least one phase error adjustment signal comprises:

generating at least one first summation error signal by taking the mean sum of the squares of a plurality of the at least one first error signals;

generating at least one second summation error signal by taking the mean sum of the squares of a plurality of the at least one second error signals; and,

generating at least one third summation error signal by taking the mean sum of the squares of a plurality of the at least one third error signals.

21. The method of claim 13, wherein the step of generating at least one phase error adjustment signal comprises:

generating at least one first summation error signal by taking the absolute sum of a plurality of the at least one first error signals;

generating at least one second summation error signal by taking the absolute sum of a plurality of the at least one second error signals; and,

generating at least one third summation error signal by taking the absolute sum of a plurality of the at least one third error signals.

22. The method of claim 17, comprising the further step of:

determining if the at least one third summation error signal is less than both the at least one first summation error signal and the at least one second summation error signal; and,

generating a phase error adjustment signal which is positive, if the at least one third summation error signal is less than both the at least one first summation error signal and the at least one second summation error signal.

23. The method of claim 17, comprising the further step of:

determining if the at least one second summation error signal is less than both the at least one first summation error signal and the at least one third summation error signal; and,

generating a phase error adjustment signal which is negative, if the at least one second summation error signal is less than both the at least one first summation error signal and the at least one third summation error signal.